1. A method comprising:

storing data at a first density in a first cell in a first memory; and

storing data at a second density in a second cell in the first memory.

2. The method of claim 1 wherein storing data at a second density in a second cell includes storing fewer bits per cell in one of said first or second cells.

3. The method of claim 1 including changing the number of bits stored per cell on the fly.

4. The method of claim 2 including storing data at levels which are spaced from one another in said cell in order to improve the read fidelity.

5. The method of claim 4 including storing data in a cell including a plurality of levels and filling less than all of said levels.

6. The method of claim 5 including storing data in regularly spaced levels within a cell while leaving intervening levels within the cell unoccupied by stored data.

7. An article comprising a medium storing instructions that enable a processor-based system to:

store data at a first density in a first cell in a first memory; and

store data at a second density in a second cell in said first memory.

8. The article of claim 7 further storing instructions that enable the processor-based system to store fewer bits per cell in one of said first or second cells.

9. The article of claim 7 further storing instructions that enable the processor-based system to change the number of bits stored per cell on the fly.

10. The article of claim 8 further storing instructions that enable the processor-based system to store data at levels which are spaced from one another in said cell in order to improve the read fidelity.

11. The article of claim 10 further storing instructions that enable the processor-based system to store data in a cell including a plurality of levels and fill less than all of said levels.

12. The article of claim 11 further storing instructions that enable the processor-based system to store data in regularly spaced levels within a cell while leaving intervening levels within the cell unoccupied by stored data.

13. A memory comprising:

a memory array including a first and second cell; and

a controller coupled to said array to store data in said array at a first density in the first cell and to store data at a second density in the second cell.

14. The memory of claim 13 wherein said memory is a flash memory.

15. The memory of claim 14 wherein said memory is a multi-level cell memory.

16. The memory of claim 13 wherein said controller stores fewer bits per cell in one of said first or second cells.

17. The system of claim 13 wherein said controller changes the number of bits stored per cell on the fly.

18. The memory of claim 17 wherein said controller stores data at levels that are spaced from one another in said cell in order to improve the read fidelity.

19. The memory of claim 18 wherein said controller stores data in a cell including a plurality of levels and fills less than all of the levels.

20. The memory of claim 13 wherein said controller stores data in regularly spaced levels within a cell while leaving intervening levels within the cell unoccupied by stored data.